1. DESIGN OF PRIORITY ENCODING BASED REVERSIBLE COMPARATORS
2. On the Analysis of Reversible Booth’s Multiplier
3. Parity Preserving Adder/Subtractor using a Novel Reversible Gate
4. A New Gate for Low Cost Design of All-optical Reversible Logic Circuit
5. Implementation of Testable Reversible Sequential Circuit on FPGA
6. A Novel Realization of Reversible LFSR for its Application in Cryptography
7. IC Layout Design of Decoder Using Electric VLSI Design System
8. Low-Complexity Tree Architecture for Finding the First Two Minima
9. Synthesis of Balanced Quaternary Reversible Logic circuit
10. Low-Power and Area-Efficient Shift Register Using Pulsed Latches
11. A Low-Power Hybrid RO PUF With Improved Thermal Stability for Lightweight Applications
12. Low Power Multiplier Architectures Using Vedic Mathematics in 45nm Technology for High Speed Computing
13. Design & Study of a Low Power High Speed Full Adder Using GDI Multiplexer
14. Design of Low Power and High Speed Carry Select Adder Using Brent Kung Adder
15. Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic
16. Design and Analysis of Approximate Compressors for Multiplication
17. Recursive Approach to the Design of a Parallel Self-Timed Adder
18. High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels
19. High-Speed, Modified, Bulk stimulated, Ultra-Low-Voltage, Domino Inverter
20. Implementation of high performance SRAM Cell Using Transmission Gate
21. Energy and Area Efficient Three-Input XOR/XNORs With Systematic Cell Design Methodology
22. Ultralow-Energy Variation-Aware Design: Adder Architecture Study
23. All Optical Implementation of Mach-Zehnder Interferometer based Reversible Sequential Counters
24. Design of Full Adder circuit using Double Gate MOSFET
25. Design of Optimized Reversible Binary and BCD Adders
27. Using Boolean Tests to Improve Detection of Transistor Stuck-open Faults in CMOS Digital Logic Circuits
28. Modeling CMOS Gates Using Equivalent Inverters
29. Reducing RMS Noise in CMOS dynamic reconfigurable latched comparator in 50 nm
30. Index-based Round-Robin Arbiter for NoC Routers
31. An Improved Dynamic Latch Based Comparator for 8-bit Asynchronous SAR ADC
32. A Novel Ternary Content-Addressable Memory (TCAM) Design Using Reversible Logic
33. A Novel Design of Reversible 2:4 Decoder
34. Design and Implementation of a Reversible Central Processing Unit
35. Performance Comparison of Pass Transistor and CMOS Logic Configuration based De-Multiplexers
36. Logic Debugging of Arithmetic Circuits
37. Reversible Logic Based Mapping of Quaternary Sequential Circuits Using QGFSOP Expression
38. A 32 BIT MAC Unit Design Using Vedic Multiplier and Reversible Logic Gate
39. Design And Development of Efficient Reversible Floating Point Arithmetic unit
40. Design and Implementation of Arithmetic Logic Unit (ALU) using Modified Novel Bit Adder in QCA
41. Quantum Cost Realization of New Reversible Gates with Transformation Based Synthesis Technique
42. Design of a Compact Reversible Carry Look-Ahead Adder Using Dynamic Programming
43. A Modified Partial Product Generator for Redundant Binary Multipliers
44. Improved Synthesis of Reversible Sequential Circuits
45. Design of Low Power, High Performance 2-4 and 4-16 Mixed-Logic Line Decoders
46. Design of reversible circuits with high testability
47. Design of high speed multiplier using Modified Booth Algorithm with hybrid carry look-ahead adder
48. Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic
49. Design of Reversible 32-Bit BCD Add-Subtract Unit using Parallel Pipelined Method
50. FTCAM: An Area-efficient Flash-based Ternary CAM Design
51. Logic Synthesis in Reversible PLA
52. Low Power Reconfigurable Hilbert Transformer Design with Row Bypassing Multiplier on FPGA
53. A Pre-Optimization Technique to Generate Initial Reversible Circuits with Low Quantum Cost
54. Primitive components of Reversible Logic Synthesis
55. Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation
56. Modeling of Adders using CMOS and GDI Logic for Multiplier Applications
57. Low-Quantum Cost Circuit Constructions for Adder and Symmetric Boolean Functions
58. Design for Testability of Sleep Convention Logic
59. Low Power High Speed Area Efficient Error Tolerant Adder Using Gate Diffusion Input Method
60. A 28 nm Configurable Memory (TCAM/BCAM/SRAM) Using Push-Rule 6T Bit Cell Enabling Logic-in-Memory
61. Design of Register File using Reversible Logic
62. A Parallel Decimal Multiplier Using Hybrid Binary Coded Decimal (BCD) Codes
63. Energy-Aware Scheduling of FIR Filter Structures using a Timed Automata Model
64. Ultra Low Voltage Synthesizable Memories: A Trade-Off Discussion in 65 nm CMOS
65. An Efficient Approach to Design a Compact Reversible Programmable Logic Array
66. Exploiting Inherent Characteristics of Reversible Circuits for Faster Combinational Equivalence Checking
GEEK WAVE SOLUTION
EMBEDDED SYSTEMS - MICROCONTROLLERS | VLSI | DSP | POWER ELECTRONICS | MATLAB PROJECTS
2012-13

IEEE Domains and Non IEEE Domains enclosed

EMBEDDED / IEEE PROJECT DOMAINS
Automatic Control * Biomedical Engineering * Broadcasting * Communications *
Consumer Electronics * Control Systems * Energy Conversion * Fuzzy Systems *
Industrial Electronics * Instrumentation and Measurement * Intelligent
Transportation Systems * Power Electronics * Power Systems * Robotics * VLSI
Systems * Wireless Communications * Micro Electro Mechanical Systems *
Mechatronics Bio Medical * Bio Metrics - Finger Print, RFID, Voice * Robotics * Security
System * Tele Communication * Communication * Unwired - Zigbee, RFID, GSM, RF,
Bluetooth, WIFI, GPS * Wired - RS232, RS485, USB, Can * Electrical * Jammers * Motors,
Drives & Controls * Networking * Power Electronics - DC to DC, Buck Boost, Inverters,
Power Factor, Converters, Harmonics & Filters, Impedance * GPS * Touch Screen *
Ultrasonic * Access Control * Intelligent Transport System * Sensors Network - Wireless
Sensors Network * Automation and Control * Automotive * Energy Management * Power
Systems * Consumer Electronics * Industrial Electronics * Encryption and Decryption * CAN
/ DAS / DCS / PLC / SCADA * Artificial Intelligence / Fuzzy Logic / Neural Networks * IVRS /
SMS * Instrumentation * Level & Analytical Instrumentation * Measurement and Control
System * Process Control * Weighing System * Mechanical * Mechatronics * MEMS *
Windmill * Solar * Thermal * Agricultural * Ethernet, USB Controllers * Digital Camera,
Satellite, Research, Photoshop, Biomedical, Copyright & Surveillance Applications * Image
Processing * Low Power Design * Power Analyzer * TTcan * VLSI Systems * Electronics *
Electrical * Communication * Hardware * Instrumentation * Mechanical * Biomedical * Tele
Communication * Automobile * Power Electronics * Power Systems
Training for students:

Initial training for students will be given for 2 Days which aids in the basic electronics components identification and various devices available in the laboratory. After this training the students will be allowed to work in the practical environment.

Practical environment and assembling methodology:

In this class students are allowed to work in the laboratory. Basic assembling training will be given to them. Assembling methodologies like forming, bending, soldering, desoldering, PCB testing, Fault identification and rectification etc. Students are practice in the instruments handling like multi meters, soldering station, SMT soldering station, CRO, computer interface testing cards, Programmer and debugger etc. After we will allow the students to assembling their projects as own.

Sensors, transducer and device exposure to students:

MEMS sensors, smoke sensor, vibration sensor, glass breaking sensor, gas leakage sensor, humidity sensor, flame sensor, intruder sensor, Temperature sensor, ECG sensor, magnetic pick up sensor, proximity sensor, accelerometer, GPS, GSM modem design, inductive type sensor, current and voltage sensor, wireless modules in range 315MHz, 433.9 MHz and 2.4 GHz, ZIGBEE module, heart beat sensor etc.

Introduction about Embedded and programming in HITECH-C and Assembly language:

The students are allowed to discuss with our engineers about an existing system design and the problem facing on the system and how to solve and enhancing the system for better performance. For this intensive training will be provided to the students, and we will teach about embedded technology, how to program in the chip and allow proper training in related language programming. After programming the microcontroller is tested in trainer kit.

Front end software design:

For student compulsory training is given the C language, then students are allowed to discuss about various languages like VB, JAVA, DOT NET and allow to select suitable language for their projects and given training to develop front tool for their project.

Final testing and explanation:

Finally the assembled hardware to interface with the computer through interface card and talk about the what are the problems we faced during the project development and how we resolve it. The explanation will be given to the students which will be extremely helpful for their viva voice and interviews.

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